AMENDMENTS TO THE CLAIMS

Claims 1-12 (Cancelled)

Claim 13 (Currently Amended): A polymer transistor arrangement, comprising:

a polymer transistor formed in and/or on a substrate including:

a first source/drain region;

a second source/drain region;

a channel region between the first and second source/drain regions;

a gate region; and

a gate-insulating layer between the channel region and a gate region; and

a drive circuit providing the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude, such that the polymer transistor has properties similar or identical to those of a Schottky diode~~source/drain regions and the gate region with electrical potentials such that a junction between at least one of the source/drain regions and the channel region is operated as a diode~~.

Claim 14 (Previously Presented): The polymer transistor arrangement as claimed in claim 13, wherein the drive circuit provides the source/drain regions and the gate

region with electrical potentials such that the junction between one of the two source/drain regions and the channel region is connected as a reverse-biased diode.

Claim 15 (Previously Presented): The polymer transistor arrangement as claimed in claim 13, wherein the channel region and the source/drain regions are produced from a material such that the junction between one of the source/drain regions and the channel region is one of a Schottky junction, an in junction, an ip junction, and a pn junction.

Claim 16 (Previously Presented): The polymer transistor arrangement as claimed in claim 13, wherein the drive circuit provides electrical potentials such that a magnitude of the gate voltage is greater than a magnitude of the voltage between the source/drain regions.

Claim 17 (Previously Presented): The polymer transistor arrangement as claimed in claim 13, wherein the junctions between respective ones of the source/drain regions and the channel region are formed geometrically asymmetrically with respect to one another.

Claim 18 (Previously Presented): The polymer transistor arrangement as claimed claim 13, wherein one of the source/drain regions is formed at least partially on the channel

region and the other source/drain region is formed at least partially below the channel region.

Claim 19 (Previously Presented): An integrated circuit arrangement having the polymer transistor arrangement as claimed in claim 13.

Claim 20 (Previously Presented): The integrated circuit arrangement as claimed in claim 19, wherein the integrated circuit arrangement is a reference voltage circuit.

Claim 21 (Previously Presented): The integrated circuit arrangement as claimed in claim 19, wherein the integrated circuit arrangement is a temperature-compensated reference voltage circuit.

Claim 22 (Previously Presented): The integrated circuit arrangement as claimed in claim 19, wherein the integrated circuit arrangement is a current source.

Claim 23 (Previously Presented): The integrated circuit arrangement as claimed in claim 19, wherein the integrated circuit arrangement is a voltage control circuit.

Claim 24 (Currently Amended): A method for producing a polymer transistor arrangement, comprising the steps of:

forming a polymer transistor in and/or on a substrate by:

forming a first source/drain region;

forming a second source/drain region;

forming a channel region between the first and second source/drain regions;

forming a gate region; and

forming a gate-insulating layer between the channel region and the gate region; and

forming a drive circuit that provides the first source/drain region with a voltage of sufficiently large magnitude and the gate region with a drain voltage of a sufficiently small magnitude, such that the polymer transistor has properties similar or identical to those of a Schottky diode~~source/drain regions and the gate region with electrical potentials such that a junction between at least one of the source/drain regions and the channel region is operates as a diode~~.